IAR Application Note 68HC12

M68HC12A4EVB hardware modifications needed for expanded narrow modes

SUMMARY

This application note describes the hardware modifications needed for expanded narrow modes. The modifications are simple, but essential.

KEYWORDS

6812, A4, M68HC12A4EVB, hardware patches, expanded narrow mode

PROBLEM

The *normal expanded narrow* or *special expanded narrow* modes cannot be used on the HC12A4EVB, or boards based on this design, without doing one or two hardware patches to the board. The modifications that need to be done to the chip select logic are simple, but essential. Without them, the CPU can only address external memory cells located on even addresses. When confronted with the problem, Motorola has neither confirmed nor denied what we believe is a hardware bug in their design.

Figure 4-3 on page 4-13 in the *M68HC12A4EVB evaluation board user's manual* shows that CPU address line A0 is used in the chip select logic for the external narrow (8-bit wide) RAM and ROM. It is obvious from the simplified schematic that for the narrow RAM/ROM devices to be selected, CS* must be asserted (CS* = 0) and A0 must be kept at a low logic level (A0 = 0). This last requirement means that all external memories will be deselected whenever A0 is high, i.e. when the CPU addresses an odd address.

SOLUTION

Fortunately, the problem is easily fixed by either connecting CS* directly to CE* and OE* of the external memories while simultaneously removing the existing connection, or by replacing A0 at the input of the OR-gate with GND. Separate OR-gates are used for the RAM and ROM chip select circuits.

If you have an HC12A4EVB and would like to use one of the narrow modes, follow these steps to patch the board using the latter alternative (replacing A0 at the input of the OR-gate with GND):

1.   Get a spare 14-pin DIP socket that fits between the U3 socket and the U3 IC (MC74HC32AN; Quad 2-input OR-gate).

Patching the external RAM chip select circuit

2a. To remove the dependency on A0, cut pin 1 of the spare socket and leave just the thick uppermost part of the pin.

2b. To connect the (former A0) OR-input to GND, solder a wire between pin 1 (the remnants of it) and pin 7 of the spare socket.

2c. Attach some isolating material to the remaining tip of pin 1 of the spare socket.

Patching the external ROM chip select circuit

3a. To remove the dependency on A0, cut pin 13 of the spare socket and leave just the thick uppermost part of the pin.

3b. To connect the (former A0) OR-input to GND, solder a wire between pin 13 (the remnants of it) and pin 7 of the spare socket.

3c. Attach some isolating material to the remaining tip of pin 13 of the spare socket.

4. Insert the spare socket between the U3 socket and the U3 integrated circuit.

With the extra modification socket in place, the board works correctly with either of the narrow modes. Please note, however, that for the board to work in normal expanded wide mode or special expanded wide mode, the socket must be removed.

CONTACT INFORMATION

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